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Robert Nally November 3, 1998

*Page 303 to Page 428*

CONDENSED TRANSCRIPT AND CONCORDANCE
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Page 303

UNITED STATES INTERNATIONAL TRADE COMMISSION
WASHINGTON, D.C. 20436
BEFORE THE HONORABLE DEBRA MORRISS
ADMINISTRATIVE LAW JUDGE
INV. NO. 337-TA-412

IN THE MATTER OF
CERTAIN VIDEO GRAPHICS DISPLAY
CONTROLLERS AND PRODUCTS CONTAINING SAME

VIDEOTAPED
ORAL DEPOSITION
OF
ROBERT NALLY
VOLUME III
November 3, 1998

Page 304

ANSWERS AND DEPOSITION OF ROBERT NALLY, Volume III, produced as a witness at the instance of the Respondent ATI Technologies, Inc., taken in the above-styled and numbered cause on the 3rd day of November, 1998, at 8:20 a.m., before Pam Durrant, a Certified Shorthand Reporter in and for the State of Texas, at the Hyatt Regency West, located at the Dallas-Fort Worth International Airport, Room 645, County of Dallas and State of Texas.

Page 305

APPEARANCES

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ATI TECHNOLOGIES, INC.

ALSO PRESENT: Mr. Dick Roach, Videographer

Page 306

INDEX

WITNESS: ROBERT NALLY, Volume III



EXHIBITS



Page 307

PROCEEDINGS
(Deposition Exhibit 22 was marked.)
THE VIDEOGRAPHER: We're on the video record 8:18, tape five.
ROBERT NALLY,
the witness hereinbefore named, having been previously duly cautioned and sworn to testify the truth, the whole truth and nothing but the truth, testified on his oath as follows:
EXAMINATION
BY MR. CORDELL:
Q. Good morning, Mr. Nally. You recall that you're under oath?
A. Yes.
Q. I'll hand you what the reporter has previously marked as Nally Exhibit 22. And for the record, it's Bates number CL 3744 through 47. And ask you to identify this, if you can.
A. It's – it's a memo to me and John Schafer from David Keene.
Q. And what does it relate to?
A. It says Patents that relate to Video mixed with Graphics.

Page 308

Q. Do you recall seeing this previously?
A. I think I saw this in the last two weeks.
Q. Okay. So you've only seen it very recently?
A. I can only recall seeing it very recently.
Q. So –
A. I cannot say I've seen it before.
Q. Certainly possible that you did. You just don't remember?
A. That's right.
Q. Do you recall ever discussing a raster ops patent with Mr. Tannenbaum or any of the patent lawyers prosecuting the 525 patent?
MR. HILL: Objection to the extent it will call for attorney/client privileged information, and I caution you not to reveal the contents of communications with your attorney for Cirrus.
A. I have no memory.
Q. (By Mr. Cordell) You just don't remember one way or the other?

Page 309

A. No.
Q. What about, do you have any memory of discussing an SPEA patent?
MR. HILL: Same objection and caution.
A. Same answer.
Q. (By Mr. Cordell) Does make it -- does make it shorter, doesn't it? I'd like you to review this briefly, if you can, and see if it jogs your memory as to whether or not you can recall discussing this.
MR. HILL: Take your time to review it, Mr. Nally.
Q. (By Mr. Cordell) Not too much time. We don't -- we don't have very long this morning.
A. I can't remember discussing really any of these patents with -- with Tannenbaum. I can't remember discussing any patents with Tannenbaum. Other lawyers, I can't remember.
Q. Now, Mr. Tannenbaum in his deposition testified that he had discussed various prior art with you. Let me -- let me read -- let me read with you -- read to you an excerpt from his deposition.

Page 310

Question -- now, this is at Page 56 of the deposition.
But what prior art was known to Mr. Nally?
Answer: I remember having a conversation with Mr. Nally. I remember sitting and asking him -- I'm not sure we did every single claim. I think we did certain claims. Maybe we did all. I just don't remember that.
I went element by element, and I asked him to think about all the prior art anybody else that he knows is doing, any of the things in there, and tell me if the combination of these anybody -- he knows anybody that's doing it or any prior art.
MR. HILL: Counsel, is there an objection to that?
MR. CORDELL: I'll -- I'll hand you the transcript, and you can read the colloquy if you'd like. But it apparently went on for a long time.
A. I can't -- I can't -- no, I can't say one way or the other. I can't remember.
Q. (By Mr. Cordell) Okay. Do you

Page 311

ever recall discussing claim elements with Mr. Tannenbaum?
MR. HILL: The same objection and instruction as before. And I note here that Mr. Jacobs instructed Mr. Tannenbaum not to reveal communications or any contents thereof.
MR. CORDELL: Well, I believe Mr. Tannenbaum did in the passage I just read, Counsel. If you read on, you'll see that there was an extensive discussion about the waiver of the privilege as is often the case in patent prosecution matters. So I think I'm entitled to find out if what Mr. Tannenbaum said is true or not.
A. I can't verify that one way or the other. I just can't remember.
Q. (By Mr. Cordell) You just don't remember whether or not you ever talked to Mr. Tannenbaum?
A. I've talked to -- I mean, we had discussions, but we had several discussions. But I can't remember what we talked about in every discussion. I can't remember which patents we talked on. I mean, I interfaced

Page 312

with him with a number of patents and -- but I don't ever remember sitting down and talking claims with him. But I ain't saying we didn't. I just don't remember it. But I can't distinguish this patent from any other patent. I can't -- you know, the meetings I had with him, I can't tell you which patents we even talked about. All I remember is sitting in the room talking with him from time to time.
Q. And I take it you also have no memory of ever discussing prior art with Mr. Tannenbaum?
MR. HILL: Same objection and instruction.
A. Yeah. I'm going to have to say I can't -- I cannot answer that question yes or no. I just don't remember.
(Deposition Exhibit 23 was marked.)
Q. (By Mr. Cordell) Let me hand you what we've marked as Exhibit 23, which for the record is CL 012 -- I'm sorry -- CL 02184 through 95. Can you identify this -- the document we marked as Nally 23?

Page 313

A. It looks like a marketing presentation.
Q. Do you recall this presentation?
A. I do not.
Q. Do you have any idea to whom it was made?
A. I have no idea who made it or who it was made to.
Q. Do you recognize the format of the slides as being associated with any particular --
A. Let me see if I can -- well, I know it wasn't me.
Q. And I take it you don't recognize these as slides one person used more often than others?
A. It's possible that one person made them and many people used them. I do not know. I mean, you know, it was a practice there at Cirrus that you put together a presentation and people kind of used that presentation or used variations of it.
MR. CORDELL: Let me have marked as Nally 24 a nine-page document entitled VESA Advanced Video Interface Committee VAVI, VIVA

Page 314

Standard Proposals Backgrounder for August 13, 1993.
(Deposition Exhibit 24 was marked.)
Q. (By Mr. Cordell) Mr. Nally, can you identify what we've marked as Nally 24?
MR. HILL: Counsel, can you give the source of this document?
MR. CORDELL: I think VESA, although I have to confess I'm not that sure.
A. It looks to me like it is the VAVI -- or the VESA VAVI proposal that came out of the VAFC committee. I'm not sure.
MR. HILL: Mr. Nally, don't speculate. If you know --
THE WITNESS: Okay.
MR. HILL: -- you know.
A. All I know for sure is it's a document that came out of VESA which is a standards committee that's a conglomerate of members of the industry.
Q. (By Mr. Cordell) Now, earlier in your deposition we discussed a subcommittee on which you served for VESA, correct?
A. Yes.

Page 315

Q. And that was the VAFC –
A. Yes.
Q. – subcommittee. The VESA advance feature connector subcommittee?
A. Yes.
Q. Did it have anything to do with the VAVI standard?
A. The VAFC, if I recall, was a subcommittee of the VAVI committee.
Q. Okay. And VAVI is VESA advanced video interface, correct?
A. Yes.
Q. Okay. Turning back to Page 6.
A. Okay.
Q. Figure 4 there offers a sample architecture for a shared memory buffer, correct?
MR. HILL: Objection. He has no personal knowledge of this document.
A. This is a bus specification, not a – not a memory specification.
Q. (By Mr. Cordell) But it is true, is it not, that there in Figure 4 there is a block entitled Shared Graphics/Video Memory?
A. Okay. Yes.

Page 316

Q. And it shows a communication line with the controller, isn't that correct?
A. Yes.
Q. And that data is then passed through the controller to the RAMDAC?
A. Yes.
MR. HILL: Mr. Nally, I caution you not to speculate on this or to give answers without reviewing this document fully.
THE WITNESS: Okay.
MR. CORDELL: Again, Counsel, I think that the witness doesn't seem to be reluctant, and I don't know why you are.
Q. (By Mr. Cordell) In the second-to-last paragraph there is a sentence that reads: The cost effectiveness and transparent integration of video and graphics have been the consequences of a single frame buffer approach in the basic architecture. Do you see that?
A. I see it.
Q. Does that have any meaning to you?
A. That were – that was the goal at the time. That's what everybody was trying to

Page 317

do, reduce cost.
Q. And the idea was that if you combined what had previously been separate video and graphics buffers, you could reduce the overall cost of the system?
A. That was the goal.
Q. Turn now to Page 7, if you will. Can you tell us whether or not Figure 5b shows a so-called video port architecture?
MR. HILL: Objection. This lacks foundation. He doesn't have any personal knowledge of this document.
Mr. Nally, I note that we have no –
THE WITNESS: Yeah.
MR. HILL: – idea what level abstraction this figure was made out of.
THE WITNESS: Yeah. That's why I –
MR. CORDELL: Counsel, let the witness testify, if you will.
MR. HILL: I'll continue to instruct my witness.
MR. CORDELL: Well, please do it in short form then.

Page 318

A. Best way to describe this is that this describes what industry – department of industry was trying to solve at the time.
Q. (By Mr. Cordell) Which was what?
A. Reducing cost by reducing dual – multiple frame buffers.
Q. So this was generally recognized in the industry at the time?
MR. HILL: Objection, vague.
Q. (By Mr. Cordell) Well, let me ask it a different way.
A. Yeah.
Q. Was it generally recognized in the fall of 1993 that reducing the cost of the system by combining the frame buffers was a good idea?
MR. HILL: Objection, ambiguous.
A. The goal – the goal here is to reduce cost. And everybody saw two frame buffers, so the goal was to try to get to one frame buffer. This was an attempt to get there. This did not say it was made. Okay?
Q. (By Mr. Cordell) My question really was whether or not that goal was generally recognized in the fall of 1993.

Page 319

A. That was recognized as a desire of – of the industry to solve that problem.
MR. CORDELL: Let me have marked as Nally 25 a document entitled – excuse me – VESA Video Interface Options, 9 February, 1993.
(Deposition Exhibit 25 was marked.)
MR. HILL: Counsel, is this our source document?
MR. CORDELL: Again, I believe it comes from VESA.
MR. HILL: Cirrus requests that you produce these documents to us.
MR. CORDELL: Well, I think I just have. I might also add, Counsel, that I have only just received these documents, but I believe that these documents have been produced as part of our regular production. I can't swear to that, but in any case, you have at least one and possibly two copies of each. Rest assured that you receive documents before I do in most cases.
MR. HILL: You mean you don't review every document?

Page 320

MR. CORDELL: Well, I mean me personally.
A. Okay.
Q. (By Mr. Cordell) Mr. Nally, have you ever seen what we've marked as Exhibit 25 before?
A. This is the first time I've ever seen this.
Q. You don't recall this ever being presented at one of your VESA meetings?
A. No.
Q. People did from time to time distribute written materials at your VESA meetings, correct?
A. Yes.
Q. Do you recall what you did with the materials you received?
A. Some of it we reviewed. Some of it was just presented and distributed, and people just didn't bother to review it.
Q. Having sat through the information and the presentation, there was no reason to review the –
A. Yeah.
Q. – written material?

Page 321

A. You had already made your decision from the presentation.
Q. Did you keep a file of your VESA activities?
A. No.
Q. Do you have any idea where the written materials that you might have received at the VESA would be today?
A. They're lost. There's – I did not keep any records at all.
Q. But chances are if you were at a VESA meeting and they had a handout, you at least –
A. Looked.
Q. – had possession of the handout?
A. Right, if I was at the meeting.
Q. Turn back to Page 5 of the document.
A. Okay.
Q. There at the top is a sample of a shared frame buffer architecture, correct?
A. No, I do not see a shared frame buffer there.
Q. Okay. Do you see a video buffer?
A. I see a RAM. I see a frame

Page 322

buffer, yes.
Q. Okay. Is it not – well, do you see a separate graphics buffer?
A. No, I do not.
Q. Do you see the title at the top of the page that says Single Frame Buffer Solutions?
A. Yes.
Q. And yet this architecture does not represent to you a single frame buffer?
A. No, it does not.
Q. Okay. Why not?
A. Because when you see the pallet, you see the eight bits going through the pallet that bypass around the pallet, it is a TrueColor bypass. That can be graphics or video data. That doesn't tell me anything about the data. That tells me there is a PseudoColor path and there's a TrueColor path. That's all it tells me.
Q. Okay. So what you're looking for here is a separate pipeline for YUV data?
A. Yes.
Q. Okay.
A. And I do not see that.

Page 323

Q. Do you see anything else that you believe to be missing?
MR. HILL: Objection, vague.
A. If they show a pallet, they should show – if there's YUV data, they should show a color converter path, a path that has color conversion. I do not see that.
Q. (By Mr. Cordell) Again, what's missing here is a backend video pipeline?
A. There is no video pipeline here at all.
Q. But you do see a backend graphics pipeline?
A. Yes.
MR. CORDELL: I now like to have marked as Nally 26 a document titled Introducing VESA Advanced Feature Connector, (VAFC), VESA Media Channel (VM-Channel), consisting of eight pages.
(Deposition Exhibit 26 was marked.)
MR. HILL: I suppose this just came to you also, Counsel?
MR. CORDELL: Well, again, I believe these have been previously produced to

Page 324

you. I will tell you that I personally have just come into possession of this.
MR. HILL: Okay.
MR. CORDELL: I don't believe that we have only recently discovered it. But the reason why it doesn't bear Bates numbers is that I just received the document.
A. Going back to this last document, I do recognize the name.
Q. (By Mr. Cordell) You do recognize the name Adge Hawes?
A. Yeah.
Q. And –
A. That's just a correction.
Q. Can you tell us who that person works for?
A. IBM.
Q. And that was in the 1993 time frame?
A. (Witness nods head.)
Q. And do you recall a presentation by, is it Mr. Hawes?
A. No. He was in the other committee. There was two committees. So I probably never saw this presentation.

Page 325

Q. What committee was he in?
A. The media – the media channel.
Q. Okay. And you were in the VAFC –
A. Yes.
Q. – committee. Okay. Turning back to Nally 26, can you identify this document for us?
A. That's – this is – looks like a presentation. The word Media Channel tells me that it came out of VESA, yeah. Let me look it over a little bit more and see what else is here.
MR. HILL: Can you read back the last question?
(The reporter read back the requested text.)
A. It is a presentation concerning the media channel and a VAFC feature connector.
Q. (By Mr. Cordell) Do you recall this presentation?
A. I do not.
Q. Do you recall anyone on the committee ever making a presentation like this?

Page 326

A. No.
Q. Turn back to Page 8.
A. Okay.
Q. And under VAVI Committee Participants, Cirrus Logic is included, correct?
A. Yes.
Q. Do you recall who attended the VAVI committee on behalf of Cirrus Logic?
A. It could have been any one of three or four people.
Q. Okay. Can you tell us who?
A. Bo Erickson, David Keene, myself. There were some others, but I don't know who they were.
Q. So it is possible that you were the delegate to the VAVI committee?
A. It's possible.
Q. Would that also include work on the VMC?
A. The VMC?
Q. The VESA media channel.
A. I had nothing to do with that.
Q. Okay. Your activities were limited only to the VAFC?

Page 327

A. Yeah.
MR. CORDELL: Let me have marked as Nally 27 a document bearing Bates numbers ATI011254 through 283.
(Deposition Exhibit 27 was marked.)
Q. (By Mr. Cordell) Mr. Nally, can you identify Exhibit 27 for us?
A. Are you asking me what I think it is?
Q. Well, can you identify it?
A. Just looking at it at this point, no, I cannot identify what kind of document. It's a document concerning a bus structure, PCI buses and such. But I can't -- I mean, just thumbing through it I can't tell if it came out of a committee, if it came out of a company or what.
Q. Well, have you ever seen this document before?
A. I can't recall seeing it.
Q. Are you aware of an effort to define a PCI multimedia specification that was ongoing in the fall of 1993?
A. There was so much going on, I

Page 328

can't say for sure that I will -- I can remember a PCI effort. There were so many efforts.
Q. Well, can you -- can you tell us what efforts you can recall, efforts to define specification?
A. Well, there's that media channel thing. It seemed like that everybody had their own proprietary solution they was trying to push.
What else was going on? I'm trying to remember. Was PCI a standard in '83 -- '93? Was it still in committee?
Q. I can tell you that I don't know --
A. Okay.
Q. -- if that helps you.
A. I was aware that there was a lot of activity in these areas. I was not involved in them. I had a different idea of my own as to how to solve these problems, and going through existing bus structures was not it, so I wasn't too concerned with any efforts in those areas so it didn't register. If it was activity, I knew about it. Just didn't

Page 329

register. I just brushed it off as this is another failed effort, this isn't going to make it so it's not worth my time.
Q. What was -- what was your approach?
A. What I call over-the-top bus.
Q. An over-the-top bus?
A. Yes.
Q. Can you describe that for us?
A. The VAFC was such an effort. The video port that we had in the 5440 was such an effort. Over-the-top bus means it's a bus that runs on a cable across the top of the ports.
Q. Providing a separate communication path between the video input and the output section of the device?
A. That's right. And now that we mention that, I do recall that there was -- Phillips was trying to do something with the PCI bus, but I don't remember anything about it.
Q. Now, the PCI bus also defined certain apertures into the device, correct?
A. I don't think PCI bus itself

Page 330

defines apertures.
Q. Well, are you familiar with the PCI bus specification?
A. One time I was.
Q. Can you turn back to Page 011267?
A. 11267.
Q. Do you see the discussion there of apertures?
A. Yes, I do.
Q. Does that refresh your recollection as to any provision for apertures in the PCI bus? I'm sorry. In the PCI specification?
A. Yeah. Is this a PCI specification, or is this a draft?
Q. Well, it says right at the top of the page Preliminary Draft Version.
A. My question is, did it make it to -- did it become part of the standard? I do not know. So I ain't going to say yes, I understand this, because I'm not -- I'm not aware of the fact that the PCI bus today defines apertures.
Q. Well, do you have any reason to doubt that this preliminary draft

Page 331

specification was distributed to at least Mr. Keene at Cirrus?
A. Yeah, I would assume that he had it.
Q. And on the front page where it says, Attached is the final print copy of the Design Guide for your information. It is being printed and will be distributed to the SIG at COMDEX.
Does that help you determine whether or not this was a -- at least a near final document?
A. I recognize -- on the front cover I recognize Dave Carson's name.
MR. HILL: Just caution you not to speculate, Mr. Nally.
THE WITNESS: Okay.
A. I recognize David Keene's name, so I know who these guys worked for at the time.
Q. (By Mr. Cordell) Who did Mr. Carson work for at the time?
A. He worked for Intel.
Q. The real basic question here, Mr. Nally, is: Are you aware of any aperturing features in the PCI specification?

Page 332

A. I'm aware of aperture features in -- I ain't going to say PCI, but in other areas. But the apertures that I was familiar with was different types of apertures. They were bit swizzle apertures. You know what I mean by bit swizzling?
Q. Big endian and little endian?
A. Big endian, little endian type stuff.
Q. If you turn the page, you can see an Endian-ness conversion.
A. Okay. Then this is -- okay. This might be where that stuff exists. Okay?
Q. I mean, turn back through the next couple of pages. You'll see a section for Aperture Implementation, Aperture Attributes, Aperture Configuration. Does any of this refresh your recollection as to the provisions for aperturing in the PCI materials?
A. Like I said, my -- I knew that they were using the term "aperture" to define swizzling. I was not concerned with this stuff. I did not get into it. And that -- at this point that's my knowledge of this spec or what Dave Carson and the PCI committee was

Page 333

doing, because I was not involved. If they were doing anything other than bit swizzling, I'm not aware of that.
But the effort at that time was to make data between the Mac and the Intel platform compatible, all compressed data compatible. In order to do that, they had to know when they looked at the data if it was big endian or little endian, and they used aperturing to solve that problem. And that's all relating to playback.
Q. So you were aware that PCI addressed aperturing at least at the level of standardizing data between the Intel and Macintosh platforms?
A. Yeah. I didn't know they made it part of the spec. I knew that there was -- to this day I don't know if that's part of the spec or not. I do not know if this ever made it.
Q. Okay.
A. That's how interested I am in PCI.
Q. Now, last night I think you committed to taking Nally Exhibit 17 home

Page 334

and --
A. Yes.
Q. -- spending some time reviewing it, so --
A. Yeah. After I relaxed I was able to read it.
Q. Good, good. I know it's -- I know it's an exciting read. I think we were discussing some of the -- some of the elements. Frankly, I can't recall exactly where we left off. So let's -- if you can flip to Page 45 under Tab 2.
A. Tab 2, Page 45. Okay.
Q. And actually flip back to Page 47. Now, there on Claim 43 the term "multi-format frame buffer" is again used, correct?
A. Yes.
Q. And you defined that yesterday as a frame buffer having I believe more than one data type in its native format?
A. That's right.
MR. HILL: Again the same objection as yesterday. Standing objection that it calls for legal conclusion. You can

Page 335

continue to ask.
Q. (By Mr. Cordell) The claim goes on to say that the multi-format frame buffer having on-screen and off-screen areas. Do you see that?
A. Yes.
Q. Can you tell us what your understanding of on-screen and off-screen areas is?
A. Any pixel in on-screen memory is viewable on the screen. By that I mean that you have a block of area in your memory that is being rastered out. The on-screen is what is being rastered through the display.
Q. Okay. Now, does that include both the -- it's hard for me to ask this question without using the terms on-screen and off-screen given your definition, so I apologize. But -- well, let me ask it this way.
Does your concept of on-screen include both graphics and video data?
A. If they are both in the same region. I mean, you can -- if you got -- as you're rastering that image out, anything in

Page 336

that area if the backend, interpret or not, it's going to go through that rastering engine.
Q. So it's really not a question of what's displayed on the -- on the CRT, but rather it's what is contained within a defined block of memory in the frame buffer?
A. Yes.
Q. So, for example, in the case where you've got video that's being rastered into the display out of off-screen memory, you would not consider that video to be an on-screen memory?
A. No.
Q. And yesterday -- and I know it was late -- but I believe you identified a start register and extent count that defined that on-screen memory portion; is that accurate?
A. That is the most common way of doing it in the industry.
Q. Okay. Is there another way?
A. Not that I know of.
Q. I mean, I guess you could define a start register and an end address rather than an extent?

Page 337

A. Yeah. That -- that is the other way. You could have a start address and an end address, and that usually compares. There's a -- there's other ways of doing it.
Q. But certainly most applications that you're aware of utilize a start address and an extent count to define the on-screen memory?
A. Yes.
Q. The claim then says, for simultaneously storing both graphics and video pixel data. Can you tell us your understanding of that phrase?
A. Simultaneously here is -- obviously you can't address two locations in memory at the same time. But by simultaneously I mean that you have free access to both.
Q. Well, there are certain dual port memories that exist, correct?
A. Yes. There's dual port memory architecture out there.
Q. For example, in VRAM?
A. Yes.
Q. Isn't it possible in VRAM to

Page 338

simultaneously store two different addresses, store data to two different addresses?
A. Once again, what do you mean by simultaneously store?
Q. Well, unfortunately what I mean doesn't count for much.
A. Well, before I answer that question I got to know what you -- what you're asking.
Q. Well, you know, you seem to offer a definition of simultaneously that's limited by practicality.
A. Yes.
Q. And I'm wondering if that limit -- if your limitation, the limitation you're imposing on the term, is reflective of the possibility that you could have a VRAM in the circuit.
A. VRAM has the same limitation as DRAM.
Q. With respect to simultaneously storing?
A. Yes.
Q. Okay. What about simultaneously retrieving?

### Page 339

A. Depends on which way you retrieve.
Q. Okay.
A. There's – memory in VRAM you add a new dimension. There is a path that is not retrieved. There is a path that is dropped and rastered.
Q. So utilizing the VRAM output port you could then simultaneously retrieve data from both active memory and out through the – through the VRAM –
A. Serial port.
Q. Serial port. Thank you. The next clause begins, circuitry for selectively retrieving. Can you tell us your understanding of that phrase?
A. I would interpret that as an addressing mechanism where elements in memory have unique addresses, and you can identify these unique elements with the address.
Q. So essentially this is a common addressing scheme wherein an address for a desired piece of data in memory is loaded into a controller, that controller then directs retrieval of that piece of data out of memory?
MR. HILL: Object to form.

### Page 340

A. If you want me to answer it yes or no, let's walk through it real slow.
Q. (By Mr. Cordell) Okay. I'm just, believe it or not, trying to put it into plain language.
A. Yeah.
Q. And I know I'm not – I'm not always going to be successful at that one. Well, let me – let me ask it on an open-ended basis.
Can you describe the mechanism whereby an address is used to retrieve a piece of data in the circuitry for selectively retrieving?
A. In other words, can I describe how a graphics controller manages its memory?
Q. Well, a little bit different question –
A. Okay.
Q. – which is circuitry for selectively retrieving.
A. Okay. Selectively retrieving in this case means that the host or it could mean – you know, what he was meaning when he wrote this I'm not sure. Selective retrieving

### Page 341

means that I can go in there and I want this pixel. I want this piece of information. I pick it up. That's what selectively retrieving means. I got a meg of memory. I want this byte. I know exactly where it's at, and I go get it.
Q. The next clause down relates to a graphics backend pipeline. I think we talked about that yesterday.
A. Yes.
Q. Do you have anything additional to add to, if you can recall, what you said yesterday about a graphics backend pipeline?
A. I can't. I'm sorry.
Q. Can you tell us what elements are in a graphics backend pipeline?
A. Okay. There is a FIFO for maintaining the raster, maintaining the stream. There – if you're retrieving multiple pixels at a time, there's got to be a serializer. There is a – if it's PseudoColor, you got what's called attributes. If it's PseudoColor, you got what's called a color lookup table to translate that into TrueColor. If you got

### Page 342

TrueColor, it bypasses all that and goes around it and goes right straight to the DAC. Both those paths, even though there's two paths there, it's all considered one pipeline in my opinion.
Q. Well, let me – let me ask you what the minimum collection of elements you would consider a graphics pipeline to consist of.
A. Okay. Be more specific. PseudoColor pipeline or a TrueColor pipeline?
Q. Well, you seem to define several options depending on the data type and whatnot. Is there a – is there a sort of a minimum version of that that you –
A. Minimum –
Q. – would still call a graphics pipeline?
A. A minimum version is TrueColor. TrueColor is a FIFO, a CRT controller which is a rastering unit, and a DAC.
Q. You would include the DAC in the graphics pipeline?
A. Yes. Because you've got to convert digital to analog at some point.

### Page 343

MR. CORDELL: Can we take just a very short break?
MR. HILL: Please.
THE VIDEOGRAPHER: We're off the video record, 9:04.
(A recess was taken.)
THE VIDEOGRAPHER: We're on the video record, 9:10.
Q. (By Mr. Cordell) Mr. Nally, can you tell us your understanding of a video backend pipeline there on Page 47?
A. What tab is that under?
Q. Well, it's under Tab 2.
A. Tab 2, okay. Okay. A video backend. You want me to describe the pipeline?
Q. Please.
A. Video pipeline, once again you got a FIFO for buffering to buffer the rastering operation. You got interpolation engine for stretching and interpolating. You got a color converter. That's it, pretty much it. And once again, you got some kind of windowing control or raster control mechanism.
Q. Well, is there a – again, is

### Page 344

there a minimum collection of elements that you would consider to be a video pipeline?
A. In this instance I have to ask – ask you a question. Is it – in what type of application? We – I mean, application for video for television is different than application for video for a computer.
Q. Okay. How about the application described in the 525 patent?
A. Okay. Minimum requirements for – for a PC is what you're saying. In my opinion minimum requirements for video pipeline for a PC application is a scaling engine and a color converter and a raster control unit – well, you have to have the whole thing.
You got to have the FIFO to buffer, because you got to buffer it because you don't know where it's going to be on the screen. You got to have the color converter because it's got to fit the windows motif. You got to have the color converter. You got to have the scaling or the interpolator to fit the windows motif, and you have the color converter to match the RGB monitor.
Q. Does the video pipeline include a

Page 345

DAC?
A. The DAC takes place after the merger of the two pipelines in this guy's case. Once you convert him to RGB, you merge him back into the graphics pipeline.
Q. Well, I thought you – I thought you identified the DAC as part of the graphics backend pipeline. Is that not true?
A. I consider that to be part of that pipeline. And what I – the way I consider it is at some point the video has got to merge with the graphics because what comes out of that backend is RGB analog data.
Q. What comes out of the graphics backend is RGB analog data?
A. That's my definition, yes.
Q. I'm just trying to understand really whether the DAC is included in the graphics backend pipeline, the video backend pipeline –
A. Well –
Q. – none of the above, all of the above. What's –
A. I'll put it to you this way. As long as I've been working with graphics,

Page 346

there's always been a DAC. So in my mind there's always got to be a DAC there.
Q. And you would put the DAC in the graphics backend pipeline?
A. Yes.
Q. And you would not put a DAC in the video backend pipeline?
A. In my definition, like I said, the video merges and back into the graphics pipeline at some point.
Q. Well, just it's a pretty plain question, Mr. Nally.
A. Yeah.
Q. Do you consider the DAC to be part of the video backend pipeline?
A. I do not.
Q. The next element is an output selector for selectively passing to said display device data received from said graphics or video backend pipelines. Do you see that? Can you tell us your understanding of that phrase?
A. Yeah. That's the MUX control or multiplexer control.
Q. And would it also include the

Page 347

multiplexer, so the output selector?
A. Yeah. That is – that is the multiplexer that selects – selectively merges the video back into the graphics pipeline.
Q. And turning back to Nally 4 –
A. Okay, okay.
Q. I take it that you would consider the frame buffer in the upper right-hand corner of the figure on Page 1 to be a multi-format frame buffer?
A. Yes, I would.
Q. You would consider that that multi-format frame buffer has on-screen and off-screen areas for simultaneously storing both graphics and video pixel data?
A. Yes.
Q. You would consider the memory sequencer to be circuitry for selectively retrieving?
A. Yes.
Q. Can you tell me what you would consider the graphics backend pipeline to be in this drawing?
A. In this drawing the graphics pipeline is kind of assumed, because this is

Page 348

an abstract proposal. And using the CLUT, that air going to the CLUT represents the – because when people seeing this document saw this, they would know what that meant.
Q. The elements in a graphic backend pipeline are very well known, correct?
A. Yes.
Q. So anyone who worked in this industry that saw this document in the fall of 1993 would know what elements were included in the graphics backend –
A. Yes.
Q. – pipeline?
MR. HILL: Objection. That called for speculation.
A. Yeah. I would – I would – to answer the question, looking at this that's the way I would interpret it.
Q. (By Mr. Cordell) Okay. And certainly you were an engineer working in the graphics industry in the fall of 1993, correct?
A. Yes.
Q. Can you tell us what the video pipeline – backend pipeline is in the figure

Page 349

on Page 1 of Nally 4?
A. What is the video pipeline?
Q. Yes.
A. It's that black block underneath everything else.
Q. Well, it's the one perhaps entitled Video Pipeline?
A. That's right.
Q. Even I picked up on that one.
A. Okay.
Q. And then finally can you point to the output selector in the figure of Page 1 of Nally 4?
A. The output selector is the two blocks, the overlay control and that little funny-looking trapezoid.
Q. And that funny little trapezoid is sort of a schematic representation of a multiplexer?
A. Yes, that's right.
Q. Okay. I'd like you to turn back now to Page 32 which is under Tab 1 in Exhibit 17. Looking at Claim 1, it reads – and you recall that anything that's struck through has been – has now been removed, so

Page 350

we can skip those words. An interface for receiving words of pixel data, each said word associated –
A. Well, what are we –
Q. – with an address –
A. Where did you start at? You said 1?
Q. Yes.
A. Oh, an interface. Okay. You started on the second line.
Q. Sorry. Well, first of all, that's a good point. Can you tell me your understanding of what a graphics and video controller is?
A. It's a controller that can store and display and manipulate both graphics data, which is RGB formatted data, or video data, which is YUV 422 formatted data.
Q. Does your understanding of the term require that it be a single chip device?
A. Well, the word "controller" implies one chip to me.
Q. So it would be your understanding that a controller that is split into two chips would not fall within this definition?

Page 351

A. No.
Q. And that would include every element set forth in this claim, correct?
A. Yes.
Q. The first limitation reads: An interface for receiving words of pixel data, each said word associated with an address buffer. Do you see that?
A. Uh-huh.
Q. Can you tell us your understanding of that phrase?
A. Yeah. That's – that's what we call a – in the industry we call it a – excuse me, I'm losing it. A write-through buffer, what it is, is the CPU, if it is writing to a controller, if that sequence or controller of that memory is busy pulling data out of that memory to send it to the – to the video or graphics pipeline, that CPU has got to wait until that memory becomes available before that write goes through.
Where if we put a buffer in there where we capture the address and the data, the CPU just more or less just posts this information in this register or this buffer.

Page 352

Goes back to what he's doing. Then the controller, when it finds the memory bandwidth, goes ahead and makes the right operation.
Q. So when you see the word "interface" you think buffer?
A. When I see the word "interface," I think interface.
Q. Okay. And that interface includes a buffer?
A. Sometimes.
Q. Can you tell me your understanding of the term "an address buffer"?
A. Yeah. The address buffer is what holds the address for that write operation, for that write-through write operation.
Q. In the system at Nally 4, can you identify for us the interface for receiving words in pixel data and the address buffer?
A. In one sentence, maintain 64 bit Alpine family compatibility. That was part of the – that's part of the 5430 product –
Q. I see. So –
A. – feature.
Q. So this element was something that

Page 353

came out of the Legacy products?
A. Yes.
Q. And by Legacy products you mean the 5430 product?
A. Yes.
Q. The next element reads, circuitry for writing each said word of said pixel data received by said interface to a one of on-screen and off-screen memory areas of a frame buffer. Do you see that clause?
A. Okay. Where? What line?
Q. Well, it starts at about Line 5.
A. Line 5, okay. Okay. I read it.
Q. And my question is: What is your understanding of that phrase?
A. For writing each said word. Well, if you're going to buffer it, you got to have a mechanism that when the memory becomes available, to go ahead and make the write operation.
Q. And is this element also part of the 5430 device?
A. Yes.
Q. Something that was just incorporated from the Legacy products?

Page 354

A. Yes.
Q. So I take it there is no explicit disclosure of it in the exhibit of Nally 4?
A. No. We – if we did anything we modified it. But I ain't going to say anything because I don't know.
Q. The next – well, before we go on – well, let's go on. The next clause reads, circuitry for selectively retrieving said words from said on-screen and off-screen areas.
Can you tell us your understanding of that phrase?
A. Yeah. That's – that's now the backend, the rastering controls. Really it's – it's the sequencer because that selective retrieving and everything is also – you can actually – that can be an I/O operation as well.
Q. So this relates to pulling –
A. Data out of memory.
Q. Okay. So and I think you testified earlier – and correct me if I'm wrong – that consists of associating an address with a particular data point and

Page 355

pulling that data point out of memory?
A. Yes.
Q. And again, I – is that feature disclosed in the – in the Nally 4 exhibit?
A. No. When – the people reading this document would know by that first line that that feature would be there.
Q. Again, that came out of the Legacy products?
A. Yes.
Q. And again, that's the 5430?
A. Right.
Q. The next clause reads, a first pipeline for processing words of graphics data retrieved from said frame buffer.
A. Yes.
Q. Can you give us your understanding of that?
A. Yeah. That's the graphics pipeline.
Q. That's the same graphics pipeline we've been talking about –
A. Right.
Q. – with respect to Claim 43?
A. Right.

Page 356

Q. A second pipeline for processing words of video data retrieved from said frame buffer is the final clause. Can you tell us your understanding of that phrase?
A. That is the video pipeline.
Q. And again, that's the video pipeline we discussed with respect to Claim 43?
A. Right.
Q. I will try my best not to be redundant because I know some of the features here are repetitive, but let's press on to Claim 2. Claim 2 begins, The controller of Claim 1 and further comprising output selection circuitry for selecting for output between graphics data received from said first pipeline and data received from said second pipeline. Do you see that?
A. Uh-huh.
Q. Can you tell us your understanding of the phrase "output selection circuitry for selecting for output"?
A. It's generating the address to identify the element in memory and pulling it out and sending it to either the video

Page 357

pipeline or the graphics pipeline.
Q. Well, let me just stop you and make sure we're all talking about the same – the same spot. This is Claim 2 –
A. Yes.
Q. – lines 2 through 5 there –
A. Yes.
Q. – where it discusses the – the output selection circuitry for selecting for output –
A. Right.
Q. – between graphics data received from said first pipeline and data received from said second pipeline. Are we talking about a memory access here, or we talking about the output section of the device?
A. (No response.)
Q. You won't be talking about the multiplexer here?
A. Are we talking about the multiplexer here?
Q. Are we?
A. No.
Q. Okay. This does – this does describe data received from the first and

Page 358

second pipeline, so that suggests at least to me that it's downstream of the first and second pipelines.
A. Okay. I see what you're saying. Let me see if you can interpret it that way.
Q. Well, I don't want to – I don't want to put words in your mouth. I really want your interpretation. I just want to make sure that you're focused on the right – right part of the claim.
A. Okay. Because I have to agree because it says received from first pipeline and received from second pipeline in a first mode data – I'm reading on down, 6, 7, 8, 9, 10. In the first mode, data pass – pass data from said first pipeline and in a second mode, pass data from second pipeline.
The operative words in there is data received from pipeline. So you're right. It is downstream from the pipelines, so I stand corrected.
Q. Okay.
A. We are talking about the MUX here.
Q. So we are talking about the MUX here?

Page 359

A. Right.
Q. Okay. And then there's the discussion of a first mode in which data is passed from said first pipeline. Well, let me read it precisely.
A. Yeah.
Q. It says, In a first mode, pass data from said first pipeline. Can you give us your understanding of that phrase?
A. Okay. A MUX has two inputs. Okay? What that is, is that's one of those inputs. Select input zero. Then you pass data from pipeline zero. In here they used one. An engineer would use the word zero.
Q. Now going back to Nally 4, I don't see an explicit disclosure of – of that first mode. Do you?
A. On this drawing here?
Q. Well, there or anywhere else on the exhibit.
A. It – if you take a look at the drawing on the front, you see that MUX right there it says, To DAC. Okay. Remember I said in my mind the graphics pipeline has multiple paths through it. You could take a look at

Page 360

that drawing called a CLUT, what I call CLUT. The arrow going from the CLUT to the MUX. And you see the other arrow going around, going to the MUX. I would consider that to be the first mode here.
Q. Because you happen to know additional details about this particular circuit?
A. Yes.
Q. But isn't it true, Mr. Nally, that, for example, the 5430 products had output selection circuitry in them?
A. Well, it selected between TrueColor and PseudoColor. But like I said, I consider that to all be part of the graphics pipeline.
Q. So you consider that a single input into the MUX?
A. Okay. So now we're going back to where I said the video taps in.
Q. Let me – let me rephrase that.
A. Yeah.
Q. What I'm getting at is –
A. Yeah.
Q. – whether or not there needed to

Page 361

be an explicit disclosure of the first and second modes set forth in Claim 2, or is this something that you as a reasonably skilled engineer would know about from your work in this area?
MR. HILL: Objection, calls for legal conclusion.
A. Yeah. I'm not that familiar with the legalese and –
Q. (By Mr. Cordell) Sure.
A. – stuff like that. I would – all I can tell you is that from my point of view – okay? – you have to specify. At some point you got to merge the video back in and that's – I mean, if you got two streams and you got one output, at some point they got to become one.
Q. Well, the 2085 had two streams, correct?
A. Yes.
Q. It could manage both video and graphics, correct?
A. Right.
Q. And it had an output MUX that combined those two streams, correct?

Page 362

A. Yes.
Q. Did the 2085 include the first and second modes described here in Claim 2?
A. Yes, it did.
Q. Could it be then that the – that the high level of abstraction in Nally 4 is not surprising given that Legacy products such as the 2085 included these first and second modes?
MR. HILL: Objection, ambiguous.
Q. (By Mr. Cordell) Answer it if you can.
A. Yeah, I don't understand –
Q. Okay.
A. – what the question. You asking me for opinion or what?
Q. In writing Nally 4 did you assume that people understood how the output MUX would work?
A. Writing this document I assumed that anybody who read it had a knowledge enough to interpret what I was trying to say in the way it was written, and obviously they were able to because they approved the program.

Page 363

Q. Well, but my question, Mr. Nally, is, you know we've pointed to Nally 4 as the document where you kind of thought of the idea.
A. Yes.
Q. And I'm looking for where you thought of the idea with respect to Claim 2, the first and second mode. I mean, and I don't find it in Nally 4 so I guess my question is, was there a later document where you had the -- you had the surprising thought to use an output MUX with two inputs?
A. No. The output MUX is there. It's in the drawing.
Q. Okay.
A. I mean, the MUX is there.
Q. Well, what about the -- a description of the first and second modes? Is that in the drawing?
A. Yeah. I mean, it's -- the drawing, you -- I can take this drawing and generate this document. Okay? That's what I'm saying. This drawing has enough information to describe what this is stating here.

Page 364

Q. Okay.
A. I see a MUX. I see a first mode. I see a graph -- you know, I see a video -- a graphics pipeline going into that MUX. Grant you, that the graphics pipeline has two arrows going into the MUX, but like I said, a graphics pipeline has multiple paths. I also see a path coming from a video pipe. That suggests to me and, you know, when I wrote this I said this is what this suggests, is that these two guys merge at this point. And I can come over here to this claim and say this is the first mode and this is the second mode.
Q. Let's now look at Claim 3, which I think now adds in a third mode to pass data -- strike that. In the third mode, pass data from said second pipeline when said data corresponds to said selected display position of said display window and data from said first pipeline match a color key.
A. Yes.
Q. Can you give us your understanding of that phrase?
A. Yeah. This is when we're

Page 365

describing the color key, capability of controlling the MUX with a color key control.
Q. I don't see a color key control in Nally 4. Am I missing something?
MR. HILL: Mr. Nally, I suggest you look on Page 2 for that question.
THE WITNESS: Picture 2?
MR. HILL: Page 2 of Nally 4.
Page 2.
THE WITNESS: Look at Page 2?
Okay.
A. Okay, okay. Claim 3 is shown two places in this document.
Q. (By Mr. Cordell) Okay.
A. On the drawing down at the bottom where it says overlay controls, you see a block called Overlay CNTL. That suggests this control circuitry. Over here in Claim 2 -- in Page 2, Roman numeral III, number 2, Digital Video Overlay, the last sentence, The overlay color key will be the only means of controlling the overlay.
Q. Let's return back to Page 1. I don't see an input into the overlay control from the graphics pipeline. Do you?

Page 366

A. Okay. You're right.
Q. And my question is not very complex --
A. Yeah.
Q. -- Mr. Nally.
A. Yeah.
Q. What I'm really looking for is, you know, was this a -- was this something new that you've added to your designs, or was this something that existed in previous parts?
A. The overlay control?
Q. Yes.
A. It was -- the concept, we already knew how to do that, yes.
Q. You knew how to do that from the 2085, for example?
A. Yes.
Q. Claim 4 now ends -- now adds in a fourth mode, correct?
A. Yes.
Q. And it reads, selection circuitry is further operable in a fourth mode to pass data from said second pipeline when data from said first pipeline match a color key.
Can you give us your understanding

Page 367

of that phrase?
A. Yeah. That means that you're looking at the color information in a graphics pipeline, and when you get -- when your color matches a certain color, you select that pixel from the video pipeline.
Q. And was this a feature that was present in the 2085 part?
A. Yes.
Q. Going on to Claim 5, it -- the additional limitation here reads, circuitry for retrieving maintains a stream of graphics data to said first pipeline and provides video data to said second pipeline when a display raster scan reaches said display position of said window.
Can you give us your understanding of that phrase?
A. Yeah. It's -- let me read it one more time just so that you don't hang me up on words here. Basically what that claim says is that the graphics data is always flowing, it's a steady stream. And to say memory bandwidth, we only pull video data when it's time to pull video data?

Page 368

Q. Well, the claim says, provides video data to said second pipeline when a display raster scan reaches a position, correct?
A. Right.
Q. Does that mean that the system does not provide video data when it -- when the raster scan is outside of the display position of the window?
A. That's what that statement says.
Q. Did the 2085 include this feature?
A. No.
Q. Is that because the 2085 didn't directly control memory? Let me ask it in a different way. What was missing?
A. 2085 had a big buffer to interface it to the video memory. 2085 had two memories, a graphics memory, a video memory. And because there were two memories and because the video memory was female, we had to drop a row and get that row staged up in advance.
Q. So I guess the distinction between Claim 5 and the 2085 has to do with the fact that you couldn't limit the video data to only

Page 369

when it was within the video window, when the raster was in the video window?
MR. HILL: Object to form.
A. The big problem was clocking. You had two memory – you had two different memory controllers. You couldn't coordinate your data, so you had to – I mean, if you're working out of one memory, you know, bang, bang, bang, bang, bang. If you're working out of two memories, you got this kind of stuff going. So you got to say I'm going to get all this stuff ready so when I get to this point. Okay?
So when you're working on two frame buffers, you got two sequencers or two memory managers, and you can't coordinate as tightly as you can if you just got one.
Q. (By Mr. Cordell) Well, but in the – and maybe we should speak with respect to the 2070 in conjunction with the 2085, so you have –
A. Yes.
Q. You have both sides of the equation there.
A. Right.

Page 370

Q. But with respect to the 2070-2085 combination, it is true, is it not, that you had a video pipeline, correct?
A. Yes.
Q. And it is also true that you had a graphics pipeline, correct?
A. Yes.
Q. And it is also true that there was a constant stream of graphic data being fed to that graphics pipeline in the 2070-2085?
A. That's true.
Q. I guess the question is: Did the system constantly feed video data to the video pipeline in the 2070-2085 combination?
A. It kept the FIFO full. It prestaged the FIFO. By that I mean we had a big FIFO in the front of the video pipeline. In order to keep that video flowing, we would preload it.
In other words, whenever we started a new frame, even if that video window was way down here at the bottom of the picture, we started a new frame. We loaded that FIFO, and that FIFO stayed loaded until it got a – when you start taking data – when

Page 371

the video pipeline started taking data out of the FIFO, you got a flag back telling the 2070, give me more data. So really you pre – that's what I call by prestaging. You prestage. You just fill that FIFO up. And when the FIFO ran down, you just kept loading it. And that was what the 2070's job was to do, was to keep that FIFO full.
Q. Isn't that exactly how the 5440 video pipeline works?
A. Not exactly.
Q. And what's the differences?
A. Number – the first difference is that there was times in the 5440 when we used the graphics pipeline to hold video data or we used a graphics FIFO to hold video data so we couldn't prestage it. We had to stage it – you know, we had to flush the video – the graphics out and load video in.
Q. But don't you have a video pipeline in the 5440?
MR. HILL: Mr. Nally, if you need to look at a 5440 spec, then you should ask for it to answer these questions.
A. The 5440 has a video pipeline.

Page 372

Q. (By Mr. Cordell) And –
A. And I probably – if we're going to talk about this, I think I do need – instead of working with my proposals. You got to remember –
Q. Sure.
A. – my proposals is not exactly what was implemented.
Q. Well, your proposal, though, is what led to the patent.
A. Yes.
Q. So we have to keep coming back –
A. Yeah.
Q. – to it.
A. Yeah, yeah. So yeah. That's what I said, if we talk about the patent. We can talk about the patent, but if we're going to use the 5440, then I need to – before I can say for sure I need to –
Q. Okay.
A. – verify what I'm going to say.
Q. There is a specification in front of you at Exhibit Number –
MR. HILL: Number 10.
MR. CORDELL: Thank you.

Page 373

Q. (By Mr. Cordell) And we have additional ones if you require them.
A. 10. I need a secretary.
MR. HILL: I'll be your secretary.
THE WITNESS: Okay.
MR. HILL: Okay?
THE WITNESS: Okay.
MR. CORDELL: He's got to be good for something.
THE WITNESS: Okay. Here we go.
A. Okay.
Q. (By Mr. Cordell) So the question is, is there a video pipeline in the 5440?
A. Yes.
Q. And does that video pipeline have a FIFO at the front end of the – of the video pipeline?
A. It has two.
Q. Two. And are those FIFOs filled in the – in the manner you've described with respect to the 2085 in that a flag is set when the FIFO gets empty and they pull more data in?
A. Yeah. There's two FIFOs, FIFO A, FIFO B. FIFO B, that's a true statement.

Page 374

FIFO A, that is not a true statement. Because FIFO A will contain either video or graphics data, depending on where you're at in your rastering line.
Q. Because FIFO A is always – always contains the line adjacent to the active line being fed into the video pipeline?
MR. HILL: Object to form.
A. Say that again.
Q. (By Mr. Cordell) Well, what is FIFO A used for?
A. FIFO A is primary to FIFO for the graphics pipeline.
Q. Where we started on this was trying to decide whether or not the 2070-2085 combination included a video pipeline that was fed with data only when the display raster was within a particular range. Can you tell me whether or not the 5440 video pipeline is fed only when the display raster is within a particular display range?
A. It depends on the operation.
Q. So I take it there is an operating mode wherein the 5440 video pipeline is fed only when the display raster is within a

Page 375

particular range?
A. There is a mode that you could do that.
Q. But there was no mode you're aware of in the 2070-2085 product wherein the video pipeline was fed only when the raster was within a particular display range?
A. Not -- not that I can remember.
Q. Turning back to Nally 4, can you show me where in the exhibit you talk about the concept of retrieving -- I'm sorry. Strike that.
Can you tell me where in Nally 4 you discuss the concept of loading the video pipeline only when the raster is within a particular address range?
A. Where do I talk about loading it only when -- okay. I'd have to read the whole document. I don't really know if it was required to specify that at this level of where this was targeted at. I mean, the people --
Q. Well, let me just --
A. I mean, let me -- this was aimed at management. Okay? I had a lot of -- you

Page 376

know, I knew what I was going to do. I didn't put everything down on this piece of paper because management is not going to want to read detail. They just want to know the meat, so this contains just the meat.
Q. So the idea about feeding the video pipeline only within a particular address range was a detail rather than meat?
A. To me that's detail.
Q. The kind of detail that you as a competent engineer would know how to implement?
A. Right.
Q. Had you ever seen that feature in other designs?
A. To me that what was novel about this design. To me that was what we was doing that I thought was so new and exciting, the ability to eliminate those big old FIFO buffers. The 2070, 2080, the Brooktree 885, those guys had huge memory buffers. What we had here was a little old bitty small buffer, reduced the cost tremendously.
Q. Well, let me make sure I'm clear about what you thought was the new and

Page 377

exciting feature.
A. One new, exciting feature.
Q. And that would be loading the video pipeline only when the --
A. Yeah. Well, reducing the size of that storage area on the chip.
Q. Okay. I understand that.
A. All right.
Q. But I thought --
A. And only -- only way you could do that was to load the video when it was time to load the video. It's not so much as load it when it's time to load the video. You feed the video in shorter bursts. That's -- see, that's the concept you're missing.
Q. Well, I'll tell you what I'm missing, Mr. Nally, is that I thought this was only one of the many operating modes of the chip.
A. Yes.
Q. And there were modes where the video was loaded all the time.
A. Well, even when it's loaded all the time, you still load it in just short bursts.

Page 378

Q. Okay.
A. You see what I'm saying? I can -- a short burst here or a short burst here, it doesn't make any difference. Okay? I'm not required to load up a whole half a line to make my system work. I only have to load up that short span to make my system work. When I load that span, all I got to do is make sure it's loaded before here. Where if I got a long span to load, I got to load it -- start loading it way over here. Where if I have a short one, if I have a small buffer, before I need the data I only have to load it at this point. If I got a buffer this wide, I got to load it from back here.
So I'm not forced to load that data -- what's the word I'm looking for? I don't have -- I'm not forced to load that data at -- I'm not restricted. Let's put it that way. I remove that restriction of you got to have that data. You have to load it. See, that's the difference. With a big buffer you have to load it. With a small buffer you don't have to load it. You don't have to load it till it's time you get there. Even though

Page 379

we loaded it and kept it loaded doesn't mean we had to.
Q. Okay. Did you ever tell the patent office that that was a -- was a good feature in the invention?
A. I figured that was what the claim was all about. I mean --
Q. The claim doesn't say anything about having the ability to load small chunks of memory.
MR. HILL: Mr. Nally, you could also refer to the specification for the patent where you disclosed all this stuff or may have disclosed the stuff.
MR. CORDELL: Yeah, he's got to testify.
A. Yeah. Once again, I never saw the patent officer. I mean, to me it was implied. It was -- you know, the claim implies that -- I mean, I don't know what you're trying to ask.
Q. (By Mr. Cordell) Well, I'm just trying to ask whether or not you ever shared with the patent office that the ability to load a small chunk of memory rather than a big

Page 380

chunk of memory was a good idea.
MR. HILL: Again, Mr. Nally, I would direct your attention to the disclosure you have made in the patent application.
MR. CORDELL: Counsel, please let him testify.
A. How do you ask this question?
MR. HILL: Counsel, I think it's a little disingenuous to --
THE WITNESS: Yeah.
MR. HILL: -- have him focus on the claims as his only disclosure to the patent office when there was a complete written description.
MR. CORDELL: You've said that three times. I mean, I think he's got the idea and --
THE WITNESS: Yeah.
MR. CORDELL: -- I think he's being forthright, and I think we should --
THE WITNESS: Yeah.
MR. CORDELL: -- we should let him. And we'll get past this and we'll go on to the next one.
THE WITNESS: Yeah, okay.

Page 381

A. We claimed a mechanism. Did a patent officer have to know the advantage it give us? That's my -- you know, that's what I'm trying to say. I covered -- I covered the capability in the -- in the claim. And my question is, do I have to tell him the marketing advantage of that in a patent? You know, this is a patent. It's not a -- when I wrote the patent, you know, that's -- I'm putting myself -- I'm trying to put myself now back into my shoes back then if I'm writing a patent.
Q. Sure.
A. I know this is an exciting feature. To me it's an exciting feature. Do I write in the patent, oh, by the way, you know, this gives us this advantage over our competitor? I've never done that in a patent before, so I didn't do it here. You go back and look at all my patents, you will never see any kind of a statement like that.
MR. HILL: Ask that last answer be stricken as nonresponsive.
MR. CORDELL: No, no. I think it was quite responsive.

Page 382

Q. (By Mr. Cordell) Okay. Well, Mr. Nally, let's try to get back to Claim 5, if we can. And we started this line discussing -- discussing where in Nally Exhibit 4 you disclosed kind of a narrow idea which was essentially turning off the video pipeline when you were outside of the -- of the video window.
Do you see that explicitly disclosed here, or is that a feature that was something you knew anybody would pick up on?
A. Don't understand where you're going to.
Q. I'm just -- I'm just trying to get back to Claim 5 where --
A. Okay, claim --
Q. -- I thought you said that --
A. Okay. Claim 5.
Q. Claim 5. It's Page 33 under Tab 1.
A. What page? Tab 2?
Q. No. Tab 1. I'm sorry.
A. Okay. Tab 1, 35. 33. Claim 5?
Q. Claim 5. I believe we were discussing the section that reads, provides

Page 383

video data to said second pipeline when a display raster scan reaches said display position of said window.
My question is really: Is that -- is that set forth in Nally 4, or is that a feature that you thought was implied or something else?
MR. HILL: Object to form.
A. Repeat the question one more time.
Q. (By Mr. Cordell) The question is: With respect to Claim 5 where it says, provides video data to said second pipeline when a raster -- I'm sorry. Let me strike that.
The question is: In Claim 5 where is says provides video data to said second pipeline when a display raster scan reaches said display position in said window, is that a feature that you disclosed in Nally 4 or not?
A. No, it was not disclosed in Nally 4.
Q. Again, you assumed that this was something that any reasonable engineer would know how to do?

Page 384

A. And remember, Nally 4 was written for management, not for engineers.
Q. Do you recall whether or not you had thought about this feature as of the writing of Nally 4?
A. Yes. I mean, I ain't going to say yes, I know for sure. I'm just saying that yes, it was the desired thing to do and I'm sure that it was on my mind.
Q. Had you seen that feature in other designs as of the writing of Nally 4?
A. No.
Q. Let's go to Claim 6.
A. Okay.
Q. The first limitation in Claim 6 reads, a video port for receiving real-time video data. Can you give us your understanding of that phrase?
A. That's saying that we put a port there to allow you to pump in live video from a VCR or something like that.
Q. Is it the VAFC port?
A. I'm -- well, it's -- let's call it the Vport. One of the modes was VAFC.
Q. And I don't see any detail in

Page 385

Nally 4 about the Vport. Is that because you understood that the VAFC port was available to anybody who wanted to use it?
MR. HILL: Object to form.
A. Implied in line Video Data down at the bottom. Do you see that?
Q. (By Mr. Cordell) Yes.
A. Implied.
Q. And again, anybody who wanted to implement a VAFC port could go to the VAFC spec and implement it, correct?
MR. HILL: Calls for speculation.
A. Yeah. I mean, what he's saying is true. I mean, it's a standard out there. I can't say you could. But, you know, I'm saying that that's speculation.
Q. (By Mr. Cordell) Well, but I mean, certainly you as a graphics engineer in the fall of 1993 could have implemented a VAFC port, correct?
A. Yes. I could have been -- let me put it this way. I could have been complied with that specification.
Q. It was -- it was known in the industry at that time?

Page 386

A. Yes.
Q. The next phrase reads, circuitry for generating an address to said memory at which said real-time video data is to be stored.
Can you give us your understanding of that phrase?
A. Yeah. That's a windowing mechanism associated with that port to allow you to generate a memory address for storing that in your frame buffer, that raster data, that real-time data coming in. Remember, you have to generate an address if you put it in memory.
Q. And we talked about this a little bit yesterday.
A. Yes.
Q. But can you tell us where that circuitry sits in the 5440?
THE WITNESS: Can I borrow that?
MR. HILL: You better look at yours.
THE WITNESS: Okay.
MR. HILL: I just note, Counsel, that this spec for the 5440 that he has is

Page 387

preliminary so might be missing some features.
A. Yeah. I would point out that that is not shown in this spec, and the reason it's not shown in this spec, because that was something done clandestine.
Q. (By Mr. Cordell) Something done clandestine meaning it was something you didn't reveal to the industry?
A. We didn't reveal to management.
Q. Reveal it to –
A. Something we did in pixel.
Q. Okay.
A. That the people in Freemont – certain people in Freemont would have had a cat so we didn't put it in the document because we knew that they were reading it.
Q. I see. Well –
A. But where it would be at would be in that block called VAFC interface.
Q. The – can you tell me when you sort of let the cat out of the bag on the Vport –
MR. HILL: Objection –
Q. – with management?

Page 388

MR. HILL: – to form.
A. I don't know exactly when, but at some point Freemont realized that that was something that needed to be there and we said "surprise."
Q. (By Mr. Cordell) You had it all along?
A. Yeah.
Q. Well, certainly Freemont would have access to your patent application, correct?
A. Yeah. But they already knew about the port at that point.
Q. So they knew about it by the time you filed your patent application?
A. Yes. Oh, yeah.
Q. Well, do you remember when?
A. When did they know about it?
Q. Yes.
A. I cannot remember. It was before we taped out. I know that.
Q. Sometime in 1994?
MR. HILL: Asked and answered.
A. I cannot answer. I mean, I was off doing other things at that point.

Page 389

Q. (By Mr. Cordell) Now, in Exhibit 10 you pointed out – you pointed to the VAFC interface as being the circuitry for generating an address.
A. That would – in this – in this drawing it would be in that area of the drawing.
Q. Let me hand you what we previously marked as Respondent's Exhibit 7 in this case which may be a more complete specification for the – well, let me ask you what it is. What is Exhibit 7?
A. Okay. It looks like the Cirrus Logic TR – I don't know what they call it, but it's what they give to their customers. It's a manual.
Q. Okay.
A. TRG or something like that.
Q. Those are publicly distributed then?
A. Yes.
Q. And what product does it relate to?
A. 543x, 4x.
Q. So this is part of the – well,

Page 390

this is the documentation for the 5430 and 5440 products?
A. Yes.
Q. And they use a single manual for both products?
A. Yes.
Q. Now, can you point out where in Exhibit 7 the circuitry for generating an address is described?
A. I'm going to have to find that in this? I've only got an hour left.
Q. Well, I'm hopeful.
A. Let's see if there is an index.
Q. I have a much larger –
A. Oh, well –
Q. – document.
A. – that might not even be in this. Because remember, this is for the customers.
Q. Uh-huh.
A. And why would we want to put this in something we give to customers because it wouldn't help the customer. It would just tell our competitors how we did what we did. Putting that in this document would not assist

Page 391

the customer in any way, so I would doubt very seriously if that information would be in this document.
Q. Let's go back to the patent then, if we can.
A. Okay.
Q. And it's – well, it's in the book in front of you.
A. Okay.
Q. It's Respondent's Exhibit 1.
A. Okay.
Q. No. Maybe 2. Can you tell me where in the patent the circuitry for generating an address sits?
A. 213, in the drawing.
Q. Now, we discussed this a bit yesterday, but I just want to make sure I'm clear. Is there any portion of the circuitry for generating an address in the host?
A. The host identifies where the window is located. In other words, you have to have a pointer. There is a block of memory that you're rastering. Okay? The host identifies that window for you with registers. There is registers in this 213

Page 392

that is programmed by the host to tell circuitry 213 how to do the rastering of this image.
Q. So the circuitry that sets those registers in 213 would be part of the circuitry for generating an address?
A. Repeat that, now.
Q. The circuitry in the host that sets the registers in 213 would be part of the circuitry for generating an address?
A. No.
Q. Why not?
A. The host – there is – the circuitry in the host has nothing to do with the circuitry here. The circuitry in the host, all it is, it's just addressing memory. It addresses this just like it addresses any other register in the device, any other device on the PCI bus. It just goes out there and says, at this address this is the value I put here.
The host, the processor itself has no knowledge of what this guy is doing. The code – the programmer knows, but the CPU, the host processor, does not.

Page 393

Q. Well, the host processor tells the controller in what ranges to store the data, correct?
A. The program does.
Q. And the program runs in the host processor?
A. Right. Now, the reason I'm getting real picky here –
Q. Please.
A. – is because there's people who would say, oh, there's an interface or there is some kind of a control mechanism between the host and this guy that's unique to this guy. There is not. Remember the host, this guy is just part of his map.
Q. Sure.
A. And all he does is execute the code.
Q. I'm just – I'm just trying to find out, to pin down what's included within the circuitry for generating an address.
A. Okay.
Q. And I'll tell you what my concern is, is that you seem to say, you know, the host sort of sets it up.

Page 394

A. Yeah.
Q. And then the controller does what the host tells it to do.
A. Yeah.
Q. And I'm not sure that the circuitry from generating an address is limited to the controller under those circumstances.
MR. HILL: Objection, mischaracterizes testimony.
Q. (By Mr. Cordell) So my question is: Is any portion of the circuitry for generating an address resident in the host either in software or as part of its processor or part of its operating sequences?
MR. HILL: And object to form. You can answer.
A. The answer is yes, we had to provide a driver to our customer that ran on the host.
Q. (By Mr. Cordell) And that driver is the thing that specifies the address range for the real-time video data received by the controller?
A. Yes. I – I mean, yeah, you got

Page 395

to program the thing. Okay? You have to have a way of programming it, yes, if that's the question.
Q. The videographer needs to change tapes, so if we can just take a short break?
A. Yeah.
THE VIDEOGRAPHER: We're off the video record, 10:13.
(A recess was taken.)
THE VIDEOGRAPHER: We're on the video record, 10:19, tape six.
Q. (By Mr. Cordell) I think we're up to Claim 7, Mr. Nally. And the –
A. What page?
Q. That's at Page 33 under Tab 1.
A. Okay.
Q. The claim adds in the following limitation, Said second pipeline includes a first – first in, first out memory for receiving data for a first display line of pixels in memory and a second first in, first out memory for receiving data from a second display line of pixels in memory.
Can you give us your understanding of that phrase?

Page 396

A. That's describing two FIFOs.
Q. And these were associated with the video pipeline?
A. That's describing the two FIFOs you see in Exhibit 10, Figure 1, FIFO A, FIFO B.
Q. And so I guess these are not necessarily limited to FIFOs associated with the video pipeline?
A. That's what I'm trying to say.
Q. You are aware of designs, are you not, wherein there are two FIFOs dedicated to the video pipeline? And by "dedicated" I mean not shared with the graphics pipeline.
MR. HILL: Don't speculate, Mr. Nally.
A. I can only – I would have to speculate to answer that.
Q. (By Mr. Cordell) Well, can you tell me – well, first of all, with respect to Exhibit 4, can you tell me where there is any discussion of FIFO A and FIFO B?
A. No. I didn't – once again, that's – that was considered – let me see if it's – that was considered detail when I

Page 397

wrote this.
Q. Are you aware of other designs that have utilized a FIFO A and FIFO B design?
MR. HILL: Objection, ambiguous.
A. I'm not. I mean, I don't make a habit of studying other people's work.
Q. (By Mr. Cordell) Turn to Figure 2 in Exhibit 2 there in the blue book which is the patent. And you know, I can give you another copy if that would make it easier.
A. Figure 2, Exhibit 2. Okay. Yeah, I got a copy of it. It's in here somewhere, isn't it? This is the same as this?
Q. It should be. You won't find the drawings.
A. Here.
MR. HILL: They're under Tab 1.
MR. CORDELL: Tab 11?
MR. HILL: 1.
A. I got it. Which drawing?
Q. (By Mr. Cordell) It's Figure 2.
A. Okay.
Q. I see a FIFO A as element 223, correct?
A. Yes.

Page 398

Q. And is that the FIFO A you were just referring to?
A. Yes.
Q. Now, the FIFO B I see is over at element 217. Is that the FIFO B you were referring to?
A. Okay. Yeah, this is the way I claimed it in the patent. In other words, I don't know if Schafer implemented this exactly the way I claimed it. But yeah, this FIFO B is the shared – it's the shared FIFO.
Q. I don't see the FIFO B, though, leading into the graphics pipeline. Am I missing something?
MR. HILL: Mr. Nally, I suggest you look at block 232 on that same drawing.
A. Okay. It does not show that I can see. 232. See if it's over here somewhere.
Q. (By Mr. Cordell) I think Counsel has directed you to 232, but that is the FIFO that at least to my eye –
A. Yeah.
Q. – that appears –
A. Yeah.
Q. – to be dedicated to graphics

Page 399

pipeline; is that right?
A. Yeah. The figure – the Figure 2 does not show what you're asking for.
Q. Okay. Do any of the other figures show what I'm asking for?
MR. HILL: Be clear what you're asking for.
Q. (By Mr. Cordell) Well, I'm asking for identification of the two FIFOs set forth there in Claim 7.
A. Right. What he's – let me clarify what you're asking for. You're asking for the path between the CRT FIFO or the FIFO feeding the graphics pipeline, where is that feeding into the video pipeline?
Q. Right.
A. Right.
Q. That is a way to think of it. What I'm really asking you for is the claim says that there are – that the video pipeline is provided with two FIFOs.
A. Right, right.
MR. CORDELL: Counsel, I really –
A. Okay.
MR. CORDELL: – would ask you to

Page 400

let the witness testify.
A. Right.
Q. (By Mr. Cordell) And the question is: Where are the two FIFOs that support the video pipeline?
A. Okay. The two FIFOs supports the video FIFO is FIFO B and FIFO A.
Q. Okay. Now, I thought you told me – and correct me if I'm wrong – but I thought you said you understood Claim 7 as requiring that the FIFOs receive a line of pixels from memory, correct?
MR. HILL: Objection, mischaracterizes prior testimony.
MR. CORDELL: He'll tell me.
Q. (By Mr. Cordell) I mean, that's what it says, right? It says a first in, first out memory for receiving data for a first line – display line of pixels in memory.
A. Okay. A FIFO is there to buffer data.
Q. Right. But does FIFO 217 receive pixels from memory?
A. Yes.

Page 401

Q. Okay. Where is the – where is the data path out of memory into FIFO B?
A. Okay. Go to Block 219.
Q. Okay.
A. Coming out – coming out of the right side you see a T. You see the T? Right underneath 201. You see it? Follow that line that goes down. It comes back around. It's input into MUX 224. The output of 224 goes into FIFO B.
Q. So it's your testimony that FIFO B and FIFO A there are the two that support the video pipeline?
A. Yes.
Q. Claim 8 recites a first – well, the additional limitation of Claim 8 reads, wherein first said display line adjacent in memory to said second display line.
A. Hang on. Let me go to Claim 8. Okay.
Q. Can you tell me your understanding of that phrase?
A. Okay. First display line adjacent in memory to second display line. That means two lines, one on top of the other. And by on

Page 402

top I mean Element 1 in this line – and this is – this is not linear memory. This is the – you call it virtual memory. Remember, memory is linear. Graphics is Cartesian, two dimensional.
Once you put that memory into a Cartesian form, the first display line, pixel 1 in the first display line is directly above pixel 1 of the second display line.
Q. There's a start of the line and a pitch and that –
A. Right.
Q. – tells you the repetitive pattern of the lines?
A. Right.
Q. But I guess my problem is there seem to be – there seems to be some stuff missing out of Claim 8. It could be that what you meant to say was you were describing the first display line adjacent memory to said second display line and then you meant to say something about them, or it could be that you meant to say that they were adjacent to one another. There seems to be a verb missing. Can you help us out?

Page 403

MR. HILL: The document speaks for itself.
A. I'd have to let it – read it the way you want to. I mean –
Q. (By Mr. Cordell) Can you –
A. – I can't speak. Anything I say would be speculation as to what I was thinking at the time or –
Q. Can you figure out what this means?
MR. HILL: Asked and answered.
A. On this you want my interpretation?
Q. (By Mr. Cordell) You would just –
A. We're just – we're describing a Cartesian memory space.
Q. So you would insert the line "is adjacent in memory" into the claim, insert the word "is adjacent"?
MR. HILL: Object to form.
A. I'm not familiar – the problem is that I have trouble reading what you guys write.
Q. (By Mr. Cordell) Don't we all.

Page 404

A. Yeah. But looking at this I would say we're saying, yeah, we're working with an XY space.
Q. Okay. Claims 9 and 10 recite some of the output selection features; is that right?
A. Okay.
Q. I don't want to spend a lot of time on these. Well, first let me just ask you, I mean, are the features set forth in Claims 9 and 10 any different from those that you used in the old 2070-2085 product?
MR. HILL: Take your time to review those features –
THE WITNESS: Yeah.
MR. HILL: – Mr. Nally.
THE WITNESS: Right.
A. I can't remember the features of the 20 – 2080. Best way I can answer is there was – that were similar. I mean, you was trying to accomplish pretty much the same thing. There's different ways of doing things. So we might have varied. We might have not, you know.
Q. (By Mr. Cordell) Let me just

## Page 405

address a couple of these then. At the handwritten Page 34 there is window position control circuitry written there. Can you tell us your understanding of that phrase?
A. That describes the – what I call the display window, a video display window.
Q. Now, it says, window position control circuitry for selectively generating a position control signal when a word of said data stream from said second pipeline falls within a display window. Do you see that?
A. Uh-huh.
Q. Can you tell us your understanding of the phrase "when a word of said data stream from said second pipeline falls within a display window"?
A. Yeah. When – when you're rastering and you go in, the raster pointer moves inside this – this frame structure of this video window.
Q. Okay. Is it – is it dependent upon the raster position or on the address of the word of said data stream from –
MR. HILL: Object –
Q. – said second pipeline?

## Page 406

MR. HILL: Objection, compound.
A. Repeat the question.
Q. (By Mr. Cordell) Is it dependent upon the raster position, or is it dependent upon the address of the word of said data stream from said second pipeline?
MR. HILL: Same objection.
A. You got to be more specific because –
Q. (By Mr. Cordell) Well –
A. – you're – it's more complicated, I think. I mean, it's – okay. Go ahead and ask your question.
Q. I'm not trying to do –
A. Right.
Q. – anything other than reflect the words in the claim and that makes it difficult.
A. Right, right.
Q. The claim says, when a word of said data stream from said second pipeline falls within a display window.
A. Okay.
Q. I'm wondering how a word from the data stream from said second pipeline can fall

## Page 407

within a display window.
A. Okay. We was tracking position by address.
Q. Okay.
A. That's basically, I think, what you're asking.
Q. That's what I'm asking. So when it says that, what it means is when an address of the word in the data stream from the second pipeline falls within a particular range?
A. Right. And that's not necessarily linear address. There's different way – there's different forms of – I mean, you talk about address, you talk about physical linear address, and you can talk about XY address. Okay?
Q. Okay. Which are we talking about here?
A. We used XY pointers, so it's XY addressing.
Q. Tell me what you mean by "word" in that phrase.
A. Word is 64 bits of data or 32 bits of data. It is a packet size of bits.
Q. Now, isn't it possible to have a

## Page 408

word then that extends both inside and outside of a display window?
A. No.
Q. The display window boundaries are always fixed at a word boundary; is that correct?
A. That's right.
Q. Jumping down to the color comparison limitation at Line 12 it reads, color comparison circuitry for comparing words of said data stream from said first pipeline –
A. Line – line – okay.
Q. – with a color key for providing in response a color comparison control signal. Is this a color key?
A. Yes.
Q. Similar to the color key used in the 2085, 207 product?
MR. HILL: Objection, ambiguous.
A. I can't answer that.
Q. (By Mr. Cordell) Why not?
A. Because I was the architect. Schafer can answer that, but I can't.
Q. Okay. Well, do you know of any

## Page 409

significant differences between the color key in the 2070, 2085 and that set forth in the patent?
MR. HILL: Objection, ambiguous.
A. I can't recall off the top of my head.
Q. (By Mr. Cordell) Color keys are pretty common elements, aren't they?
A. Yeah, it's pretty straightforward.
Q. I mean, you didn't set forth the details of the color key in the exhibit of Nally 4, correct?
A. No.
Q. Now, let's jump into Claim 10 quickly. Claim 10 begins with, window position counters operable to increment from initial count values corresponding to a starting pixel of the display window as data representing each pixel in a display screen is pipelined through said overlay control circuitry.
Can you give us your understanding of that phrase?
A. That's describing the addressing mechanism – I mean the pointers. I said we

## Page 410

used XY pointers. That's the way the pointer – the pointer is incremented.
Q. What is your understanding of the phrase "as data representing each pixel on the display screen is pipelined through said overlay control circuitry"?
A. Pretty much what it says. I mean, there is a pipeline and there's pixels flowing through it and –
Q. Well –
A. – and each one of those pixels is addressable. Right?
Q. When you say that it is pipelined, can you have a pipeline through the overlay control circuitry?
A. It all depends on what your definition of pipeline is. You have to latch data, stabilize the data. You got a multiplexer. If you got a – if you have a color key, then you have to look at the graphics data in advance.
So you have to have – looking at – looking at pixel – this is your pipeline here. Pixel A, Pixel B, Pixel C. You have to make a – if you use an overlay,

Page 411

during Stage B you got to look at the color at Stage A. So that constitutes to me a pipeline.
Q. Okay. So your understanding of a pipeline is a collection of sequential elements?
A. Yes.
Q. The next limitation reads, screen position counters operable to count as data representing each pixel in said display screen is pipelined through said overlay control circuitry.
Can you give us your understanding of that phrase?
A. That's – that's the pointers of the CRT controller.
Q. And then there's comparison circuitry recited there at the end of Claim 10. Do you see that?
A. Yes.
Q. Can you give us your understanding of the comparison circuitry?
A. Yeah. We – remember I said we got pointers. We got the video window pointers, and we got the screen pointers.

Page 412

What we're doing is looking for count values to tell us when we're counted to the point. So it's still comparison circuitry. We set a pointer here and we're counting. When we hit that point, we're comparing for that point.
Q. Pretty standard display stuff?
MR. HILL: Objection, ambiguous.
Q. (By Mr. Cordell) I mean, Mr. Nally, virtually every –
A. Yeah.
Q. – display system that you know of employs this pointer and counter sequence?
MR. HILL: Same objection.
A. Okay. CRT controllers, yes. Compare the circuitry, I mean, we got to remember, CRT control has been around for a long time. But when you start window inside – was people doing this at that time? I don't know. Today it is commonplace. Back then I can't say yes. But today, yes.
Q. (By Mr. Cordell) Okay. Let's see if we can't pick up the pace here. Can you turn now with me under Tab 10, Page 49, Claim 13. Let me just touch on a few of these elements.

Page 413

Refer down to the limitation second from the bottom in Claim 13 that reads, video backend pipeline for processing other ones of said words of data representing video data retrieved from said frame buffer. Do you see that?
A. Uh-huh.
Q. Can you give us your understanding of that phrase?
MR. HILL: I believe we went through this yesterday.
MR. CORDELL: Well, we went through a portion of this yesterday, but the witness was a little tired and I don't want to –
MR. HILL: I understand.
A. Okay. Do I have to read up front to see what they mean by "other ones"?
Q. (By Mr. Cordell) Well, you certainly can, yes.
A. Okay. What – let me see. It says that we're able to handle different formats of video data.
Q. What are the possible formats of video data in the 525 patent?

Page 414

A. 422, 444, PackJR. I can't remember if we implemented some of the other formats in this one or not. I think in the 46 we did other formats, but in the first one I don't know if we did any other than those.
MR. HILL: Just caution you, Mr. Nally, if you need to be certain on this you need to –
THE WITNESS: All right.
MR. HILL: – look at the specification of the patent and see what you put in there.
A. Well, we're talking about the 5440, not the patent. And you said what was in the 5440, right?
Q. (By Mr. Cordell) Well, I think I said the patent, but I'll take the 5440.
A. Okay.
Q. I'll take whatever you can give me.
A. Well, in the patent we did not – I don't think we claimed any format in particular. I'm not sure.
MR. HILL: Don't speculate, Mr. Nally.

Page 415

THE WITNESS: Okay.
MR. HILL: Be sure.
THE WITNESS: Okay.
A. I don't recall how many we claimed off the top of my head.
Q. (By Mr. Cordell) Now, further down in the same clause it reads, said circuitry for retrieving always rastering a stream of data from said frame buffer to said graphics backend pipeline.
Can you give us your understanding of that phrase?
A. Where are you at? Is this on the same page?
Q. Yes.
A. I put selecting for output between –
Q. Well, not quite that far down. It said, Circuitry for retrieving always rastering a stream of data from said frame buffer to said graphics backend pipeline.
A. Okay. Was – okay. Just that phrase right there, circuitry for retrieving always –
Q. Right.

Page 416

A. – rastering a stream.
Q. That's right.
A. Okay. That means that we had the – to keep the graphics pipe always going.
Q. In the next – well, do you mean that the graphics pipe was always going, or do you mean you were always retrieving words – a stream of data?
MR. HILL: Object to form.
A. It means we was keep – we was trying to keep the graphics pipelines FIFO full.
Q. (By Mr. Cordell) Is there different – is there a difference between rastering a stream of data and rastering words of data?
A. No.
Q. And again, these words are 32 bit words?
A. Yes.
Q. Packets?
A. A word can be depending, you know, 32 or 64. Some products they were 32. Some products they were 64.
Q. Okay. But what you mean to imply

Page 417

there is a collection of pixels that are packaged up into some manageable size?
A. Yes.
Q. How many pixels are there in a 32 bit word if you have 8 bit graphics data?
A. Four.
Q. How many words are there in a 64 bit – strike that.
How many pixels are there in a 64 bit word if you have 8 bit graphical video?
A. Eight.
Q. Strike that whole thing. Let me try one more time. How many pixels do you have in a 64 bit word when you have 8 bit graphics data?
A. Okay. Eight.
Q. And the way you do that is 64 divided by 8 gives you 8?
A. Right. Trouble with the math, right?
Q. I'm trying to hurry. That's the problem.
Now, the final limitation of the clause we've just been discussing reads, And rastering video data to said backend – I'm

Page 418

sorry. And – strike that.
The final clause reads, And rastering video data to said video backend to pipeline when a display raster scan reaches a display position of a window.
Can you give us your understanding of that phrase?
A. Yes. The display – the video display window can be anywhere on the screen, and you raster that display on the top left. Okay? As you raster along, at some point you're going to hit that first pixel in that window. That's what we're describing here is the circuitry. Let's see.
Video data said backend pipeline when a display raster scan reaches a display window of a screen. In other words, we kick on that pipeline when we know we're at the window.
Q. So you would – you would say that this phrase means that you feed the video pipeline only when you're within that window?
A. I would say that we enable the feeding at that point. I ain't saying that's the only point we enable it. I'm saying

Page 419

that's the crucial point for enabling that feed.
Q. That's really the question. The question is: Does this also include the case where you're always feeding the video pipeline?
A. Well, number one, if you've got a small window of video and a big rastering, it's impossible to always feed that video because you can't display it until you get to that point. Okay? You follow what I'm saying?
Q. Uh-huh. But you do always feed the graphics pipeline, correct?
A. Yes.
Q. Even when you're not displaying it?
A. What do you mean by that? You're going to have to be more specific. What do you mean –
Q. Well –
A. – by that statement?
Q. In the construct of Claim 13 you feed the graphics pipeline even when you are with – when the raster is within the video

Page 420

window, isn't that true?
A. That's one of the modes.
Q. And that's the mode being discussed in Claim 13?
A. Yes.
Q. And my question is: In Claim 13 is it also true that the video window is always being fed? I'm sorry. Strike that.
In Claim 13 is it also true that the video pipeline is always being fed even when the raster is outside of the video window?
A. What do you mean by being fed?
Q. Well, I mean – let me ask it this way. Is it true in the mode of Claim 13 that the system rasters video data to the video backend pipeline when a display raster scan is outside a display position of a video window?
A. Okay. There's – there's no reason for it not to. But then again, when you fill up the FIFO the mechanism cuts off automatically. So even if you were rastering outside the window, there is a limited amount of rastering you can do. Once the FIFO fills up, the fetches from the memory stops until

Page 421

the FIFO well is empty.
Q. And so there's no more rastering in your opinion?
A. Well, once again, we go back to the definition of rastering. At that point you're not even rastering in the video window. You're rastering outside the video window. So if you're rastering outside the video window, the video pipeline, FIFO – the video pipeline could be dormant because there's no mechanism driving it.
Q. Well, but now there are two kinds of rastering that we've discussed. One is rastering on the screen. The other is rastering out of memory. Remember the rastering out of memory discussion?
A. Okay.
Q. And this, I think, relates to the rastering out of memory. I understand that's imprecise, but that's what's in the claim so –
A. Okay. I see – okay. You – I see where you are. Okay. Now I see what you're trying to say. Okay. Let me look at it from that point of view.

Page 422

MR. HILL: Just want to point out the time, Counsel, in case you want to wrap up.
MR. CORDELL: I'm hurrying. I am hurrying.
MR. HILL: What's the present question?
A. Okay. Anytime I see the word "rastering" and "backend" in the same sentence, that implies to me that you're driving a rastering display device. So to me when you say rastering out of memory and rastering to the display, it's the same operation, just saying it two different ways.
Now, to clear up what I mean is a bit operation is a raster operation as well, but there is no backend involved. So that's the reason why I want to make it clear that you understand that rastering out of memory – rastering to a display, that rastering out of memory in this definition is tied to a rastering for display because backend is in the sentence.
Q. Okay. But certainly the rastering to a display is a continuous operation,

Page 423

correct?
A. Yes.
Q. I mean, one pixel follows the next and there's a pitch or –
A. Right.
Q. – a delay between pixels 140 nanoseconds or something. But one follows the next over –
A. Right.
Q. – and over and over again?
A. Right.
Q. And I thought you described the operations out of memory as being more bursty than that.
A. Yes.
MR. HILL: Objection, mischaracterizes prior testimony.
MR. CORDELL: I think the witness disagrees with you but –
Q. (By Mr. Cordell) So I'm having a hard time using the term "rastering" to describe the memory sequence unless there's something else going on.
A. Okay. Let's change our wording then. Okay? Just during a raster to display,

Page 424

you're bursting out of memory to fill your FIFO so that you can raster from your FIFOs to the display.
Q. Okay. But that's – that's rastering out of the FIFOs as opposed to rastering out of the memory, correct?
MR. HILL: Object to form.
A. To me it's all part of the same mechanism.
Q. (By Mr. Cordell) Okay. Let me – my watch is about to go off, so let me ask you this question. Are you aware of any – do you know what the term "prior art" means?
A. Yes.
Q. Are you aware of any prior art that we have not discussed during your deposition?
MR. HILL: Objection, calls for legal conclusion and possible expert testimony. Go ahead and answer.
A. Prior art in what sense?
Q. (By Mr. Cordell) Well, I thought you told me you understood what the term "prior art" meant.
A. Right. What I'm – are you

Page 425

talking about prior art about –
Q. I'm talking about prior art that includes –
A. Be more specific.
Q. – the elements of the claims of the 525 patent.
A. Oh.
MR. HILL: Same objection.
A. If I did I would have claimed them at the time. I mean, I would have –
Q. (By Mr. Cordell) Well, I'm really asking you a different question. Here today do you know of any prior art –
A. Oh.
Q. – in the 525 patent that we have not discussed during your deposition?
MR. HILL: Same objection.
A. I feel very comfortable in saying I doubt it.
Q. (By Mr. Cordell) Okay. Did you undertake to search through your personal files for prior art relating to the 525 patent?
A. Before or after or when?
Q. At any time.

Page 426

A. My personal files?
Q. Yes.
A. Let's go back. State that –
Q. Okay. At any time have you undertaken a search of your personal files to determine whether or not you have any prior art relevant to the 525 patent?
MR. HILL: Same objection.
A. I'm not sure what you're asking. But number – number one, any files I have today are TI property. Had nothing to do with back then. So when I left Cirrus it was all history. So I don't know where we – what you're really asking for here.
Q. (By Mr. Cordell) What I'm really asking is whether or not you've looked through your personal files, either the ones you have at TI or the ones that you have at home or anyplace, to see if you have a prior art to the 525 patent.
MR. HILL: Same objection.
A. Number one, I don't have such files of keeping records of what other people are doing.
Q. (By Mr. Cordell) Well, you

Page 427

certainly have papers and brochures and things that reflect other people's products, correct?
MR. HILL: Object to form.
Q. (By Mr. Cordell) Let me just ask you to do it. Would you mind searching through your files both at work and at home to see if you have anything that relates to the elements of the claims in the 525 patent, and if you find them can you give them to Mr. Hill?
A. Yeah, I can do that because I don't keep files like that.
Q. But I want you to look.
MR. HILL: Let me just say we've already asked Mr. Nally to search through his –
THE WITNESS: So I –
MR. HILL: – whatever he has, and I've got what we got.
MR. CORDELL: Plan to take your deposition at some point. I just don't know when. Okay. I don't know why my watch didn't go off, but I now have 11:01. The witness – for the convenience of the witness, we're

Page 428

going to adjourn now. We will make every effort not to call you back, but if we have to we will.
THE WITNESS: Thank you, sir.
MR. CORDELL: Thank you, Mr. Nally.
THE VIDEOGRAPHER: We're off the video record, 11:04.
- - - - -

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--0--

011267 [1] 330:5
012 [1] 312:23
02184 [1] 312:23

--1--

1 [19] 347:9; 349:1, 12, 22, 23; 350:7; 356:14; 365:23; 382:20, 22, 23; 391:10; 395:15; 396:5; 397:17, 19; 402:1, 8, 9
10 [11] 358:15; 372:24; 373:3; 389:2; 396:5; 404:4, 11; 409:14, 15; 411:19; 412:23
10:13 [1] 395:8
10:19 [1] 395:11
11 [1] 397:18
11267 [1] 330:6
11:01 [1] 427:24
11:04 [1] 428:8
12 [1] 408:9
13 [8] 314:1; 412:24; 413:2; 419:23; 420:4, 6, 9, 15
140 [1] 423:6
17 [2] 333:25; 349:23
19 [1] 428:15
1993 [9] 314:2; 318:14, 25; 319:6; 324:18; 327:24; 348:10, 21; 385:19
1994 [1] 388:22
1998 [2] 303:18; 304:6

--2--

2 [27] 334:12, 13; 343:13, 14; 356:13; 357:4, 6; 361:2; 362:3; 363:7; 365:6, 7, 8, 9, 10, 18, 19; 382:21; 391:12; 397:7, 8, 11, 21; 399:2
20 [1] 404:19
20005 [1] 305:16
201 [1] 401:7
20436 [1] 303:2
207 [1] 408:19
2070 [4] 369:20; 371:3; 376:20; 409:2
2070's [1] 371:7
2070-2085 [6] 370:1, 10, 14; 374:15; 375:5; 404:12
2080 [2] 376:20; 404:19
2085 [14] 361:18; 362:2, 8; 366:16; 367:8; 368:11, 13, 16, 17, 24; 369:20; 373:21; 408:19; 409:2
213 [5] 391:15, 25; 392:2, 5, 9
217 [2] 398:5; 400:23
219 [1] 401:3
22 [3] 306:11; 307:2, 17
223 [1] 397:23
224 [2] 401:9
23 [4] 306:12; 312:19, 22, 25
232 [3] 398:16, 18, 20
24 [4] 306:13; 313:24; 314:3, 6
25 [4] 306:14; 319:4, 7; 320:5
26 [4] 306:15; 323:16, 20; 325:6
27 [4] 306:16; 327:3, 5, 8
283 [1] 327:4

--3--

3 [3] 303:18; 364:15; 365:12
307 [2] 306:5, 11
312 [1] 306:12
314 [1] 306:13
319 [1] 306:14
32 [6] 349:22; 407:23; 416:18, 23; 417:5
323 [1] 306:15
327 [1] 306:16
33 [3] 382:19, 23; 395:15
337-TA-412 [1] 303:5
34 [1] 405:2
35 [1] 382:23
3744 [1] 307:18
3rd [1] 304:5

--4--

4 [28] 315:15, 23; 347:5; 349:1, 13; 352:17; 354:3; 355:4; 359:15; 362:6, 17; 363:2, 9; 365:4, 8; 366:18; 375:9, 13; 382:5; 383:5, 19, 22; 384:1, 5, 11; 385:1; 396:21; 409:12
422 [2] 350:18; 414:1
425 [1] 305:6
43 [3] 334:15; 355:24; 356:8
444 [1] 414:1
45 [2] 334:12, 13
46 [1] 414:3
47 [3] 307:19; 334:15; 343:11
49 [1] 412:23
4x [1] 389:24

--5--

5 [14] 321:17; 353:12, 13; 357:6; 367:10; 368:24; 382:2, 15, 18, 19, 23, 24; 383:11, 15
525 [9] 308:16; 344:9; 413:25; 425:6, 15, 23; 426:7, 20; 427:9
5430 [6] 352:22; 353:4, 22; 355:11; 360:11; 390:1
543x [1] 389:24
5440 [16] 329:11; 371:9, 14, 21, 23, 25; 372:18; 373:13; 374:19, 24; 386:19, 25; 390:2; 414:14, 15, 17
56 [1] 310:2
5b [1] 317:8

--6--

6 [4] 315:13; 358:14; 384:13, 15
601 [1] 305:15
64 [8] 352:20; 407:23; 416:23, 24; 417:8, 10, 14, 17
645 [1] 304:10

--7--

7 [8] 317:7; 358:14; 389:9, 12; 390:8; 395:13; 399:10; 400:10

--8--

8 [11] 326:2; 358:14; 401:15, 16, 19; 402:18; 417:5, 10, 14, 18
83 [1] 328:13
885 [1] 376:20
8:18 [1] 307:5
8:20 [1] 304:6

--9--

9 [4] 319:5; 358:14; 404:4, 11
93 [1] 328:13
94105-2482 [1] 305:7
95 [1] 312:24
9:04 [1] 343:5
9:10 [1] 343:8

--A--

a.m. [1] 304:6
ability [3] 376:19; 379:9, 24
able [3] 334:5; 362:24; 413:22
above-styled [1] 304:4
abstract [1] 348:1
abstraction [2] 317:17; 362:6
access [3] 337:18; 357:15; 388:10
accomplish [1] 404:21
accurate [1] 336:18
active [2] 339:9; 374:6
activities [2] 321:4; 326:24
activity [2] 328:19, 25
add [3] 319:16; 339:3; 341:12
added [1] 366:9
additional [5] 341:11; 360:7; 367:11; 373:2; 401:16
address [42] 336:24; 337:2, 3, 6, 15; 339:19, 21; 340:12; 350:5; 351:7, 23; 352:13, 14, 15, 19; 354:25; 356:23; 375:16; 376:8; 386:3, 10, 13; 389:4; 390:9; 391:14, 19; 392:6, 10, 20; 393:21; 394:6, 13, 22; 405:1, 22; 406:5; 407:3, 8, 12, 14, 15
addressable [1] 410:12
addressed [1] 333:13
addresses [5] 338:1, 2; 339:18 392:17
addressing [5] 339:17, 21; 392:16; 407:20; 409:24
adds [3] 364:16; 366:18; 395:7
Adge [1] 324:11
adjacent [7] 374:6; 401:17, 23 402:20, 23; 403:19, 20
adjourn [1] 428:1
ADMINISTRATIVE [1] 303:4
advance [3] 315:3; 368:22; 410:21
Advanced [2] 313:25; 323:17
advanced [1] 315:10
advantage [3] 381:2, 7, 17
agree [1] 358:11
aimed [1] 375:24
ain't [6] 312:3; 330:20; 332:2; 354:5; 384:6; 418:24
air [1] 348:2
Airport [1] 304:10
allow [2] 384:20; 386:9
Alpine [1] 352:21
ambiguous [6] 318:17; 362:10; 397:4; 408:20; 409:4; 412:7
amount [1] 420:23
analog [3] 342:25; 345:13, 15
Answer [2] 310:5; 362:11
answer [15] 309:6; 312:17; 338:7; 340:1; 348:17; 371:24; 381:22; 388:24; 394:17, 18; 396:18; 404:19; 408:21, 24; 424:20
answered [2] 388:23; 403:11
ANSWERS [1] 304:1
answers [1] 316:9
anybody [7] 310:13, 15, 16; 362:21; 382:11; 385:3, 9
anyplace [1] 426:19
Anytime [1] 422:8
anywhere [2] 359:19; 418:9
Aperture [3] 332:16, 17
aperture [2] 332:1, 21
apertures [8] 329:24; 330:1, 8, 11, 23; 332:3, 4, 5
aperturing [4] 331:25; 332:19; 333:10, 13
apologize [1] 335:19
apparently [1] 310:21
APPEARING [2] 305:8, 17
appears [1] 398:23
application [8] 344:5, 7, 8, 13; 380:4; 388:10, 15
applications [1] 337:5
approach [2] 316:20; 329:5
approved [1] 362:24
architect [1] 408:23
architecture [6] 315:16; 316:20; 317:9; 321:21; 322:9; 337:22
area [5] 335:12; 336:1; 361:5; 377:6; 389:6
areas [8] 328:19, 24; 332:3; 335:4, 9; 347:14; 353:9; 354:11
aren't [1] 409:8
arrow [2] 360:2, 3

--N--



--O--

--W--



--X--



--Y--



--Z--

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